REMARKS

Claims 1-17, 19, and 20 remain pending. Claims 1-10, 15, 16, and 17 have been amended to clarify the invention.

The Examiner has objected to claims 3 and 8 because of informalities. Claim 3 and 8 have been amended to correct these informalities.

The Examiner has rejected claims 15-17 under 35 U.S.C. §102(e) as being anticipated by Muller et al. (U.S. Patent No. 6,044,087). The Examiner has also rejected claims 1-10 and 19-20 under 35 U.S.C. §103(a) as being unpatentable over Muller et al. in view of Official Notice. Claims 111-12 are rejected under 35 U.S.C. §103(a) as being unpatentable over Muller et al. in view of Lese et al. (4,761,800), and claims 13-14 are rejected as being unpatentable over Muller et al. in view of Chow et al. (6,169,742). The rejections are respectfully traversed for at least the following reasons.

Claim 1 is directed towards a "method of communicating between a media access control layer and a physical layer." Claim 1 also requires "sending a plurality of time-division multiplexed receive control signals on a single receive control pin" and "sending a plurality of time-division multiplexed transmit control signals on a single transmit control pin." Claim 1 also requires "wherein the receive control signals include a receive data valid signal and a receive error signal and the transmit control signals include a transmit enable signal and a transmit error signal." Independent claim 15 is directed towards an "interface between a first media access control layer and a second media access control layer." Claim 15 also requires "a time-division multiplexed receive control pin for transmitting different functional types of receive control signals including a receive data valid signal and a receive error signal" and "a time-division multiplexed transmit control pin for transmitting different functional types of transmit control signals including a transmit enable signal and a transmit error signal." Independent claim 16 has similar elements. In other words, mechanisms are provided for receiving the receive data valid signal on the same single pin as the receive error signal and for transmitting the transmit enable signal on the same single pin as the transmit error signal.

Although the primary reference Muller et al. teaches multiplexing of certain signals onto a same pin, the transmit enable signal is not transmitted on the same pin as the transmit error signal. Likewise, Muller et al. fails to teach that the receive data valid signal is received onto the same pin as the receive error signal. In contrast, Muller shows that these signals are transmitted or received on separate pins. Muller teaches that the set of signals TxD0, TxD1, and TxD3 are multiplexed with the set of signals TXD3, TXEN, and TXER so that the first set transmits during

the first half of the clock cycle, while the second set transmits during the second half of the clock cycle. See Fig. 3b. However, the signals from each set are individually transmitted on three separate output pins 309. See Fig. 3a. Likewise, the set of signals RxD0, RxD1, RxD3 are received during the first half of the clock and the set of signals are RxD3, RxDv, and RxER are received during the second half of the clock cycle. Fig. 4b. However, the signals from each set are individually received onto three separate output pins (unlabeled). See Fig. 4a. Furthermore, Muller et al. lists the signals which are multiplexed as being TxD0 with TxD3; TxD1 with Tx_EN (transmit enable); TxD2 with Tx_ER (transmit error); RxD0 with RxD3; RxD1 with Rx_DV (receive data valid); and RxD2 with Rx_ER (receive error). See Col. 6, Lines 33-42. In other words, although the transmit enable Tx_EN is multiplexed with data bit TxD1, it is not multiplexed with the transmit error Tx_ER. Likewise, although the receive data valid Rx_DV is multiplexed with data bit Rx_D1, it is not multiplexed with the receive error Rx_ER, in the manner claimed. The secondary references also fail to teach such multiplexing of signals in the manner claimed.

In sum, the cited references fail to teach or suggest receiving the receive data valid signal on the same control pin as the receive error signal and transmitting the transmit enable signal on the same control pin as the transmit error signal, in the manner claimed. Accordingly, it is respectfully submitted that claims 1, 15, and 16 are patentable over the cited reference.

The Examiner's rejections of the dependent claims are also respectfully traversed. However, to expedite prosecution, all of these claims will not be argued separately. Claims 2-14, 17, and 19-20 depend directly or indirectly from independent claims 1 or 16 and, therefore, are respectfully submitted to be patentable over cited art for at least the reasons set forth above with respect to claims 1 or 16. Further, the dependent claims require additional elements that when considered in context of the claimed inventions further patentably distinguish the invention from the cited art.

Applicant believes that all pending claims are allowable and respectfully requests a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

Respectfully submitted,
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